15EC53

Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020 Verilog HDL

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

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		Module-1	(06 Montra)	
1	a.	Explain the advantages of HDL's over schematic-based design.	(06 Marks)	
	b.	Explain top-down design methodology and bottom-up design methodology.	(10 Marks)	
	OR			
2	•	Discuss the trends in HDLs.	(06 Marks)	
2	a. b.	Explain the design hierarchy using 4-bit ripple carry counter.	(10 Marks)	
	υ.	Explain the design incrarchy using 4-our ripple carry counter.	(10 1/11/115)	
	Module-2			
3	a.	Explain the following data types with an example in verilog:		
,	и.	i) Vectors ii) Registers iii) Time iv) Real.	(08 Marks)	
	b.	What are system tasks and compiler directives? Explain.	(08 Marks)	
		OR		
4	a.	What are the components of SR-latch? Write verilog HDL module of SR-latch.	(08 Marks)	
	b.	With an example, explain Hierarchical names.	(08 Marks)	
		7 10 6		
		Module-3		
5	a.	With the help of logic diagram, write a verilog code for 4 to 1 multiplexer using g	ate – level	
		modeling.	(08 Marks)	
	b.	What are rise, fall and turn-off delays? Explain, how they are specified in verilog.	(08 Marks)	
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		OR	(06 Marks)	
6	a.	Explain conditional and concatenation operator with an example.	(06 Marks) (10 Marks)	
	b.	Write a verilog dataflow description for 4-bit full adder with carry lookahead.	(10 Marks)	
		Module-4		
-		Explain briefly event based timing control in verilog.	(08 Marks)	
7	a.	Explain sequential and parallel blocks of verilog HDL.	(08 Marks)	
	b.	Explain sequential and paramet blocks of verilog 11DE.	(001,201,115)	
		OR		
8	a.	Write a verilog HDL code for JK flip-flop using case statement.	(08 Marks)	
Ů	b.	With syntax, explain conditional and branching loop statements in verilog HDL.	(08 Marks)	
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		Module-5		
9	a.	Explain the advantages and benefits of VHDL.	(06 Marks)	
	b.	Write a VHDL code for full-adder using two half adder in mixed style description		
			(10 Marks)	
	OR			
10	a.	Explain the synthesis process with a block diagram.	(10 Marks)	
10	b.	Differentiate between signal assignment and variable assignment.	(06 Marks)	
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Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.